Subhajit Paul

test.dev.paul@gmail.com | +91 8420344070 | subhajit-paul.github.io

Research Interests

I am interested in Electronic Design Automation (EDA) and Large Language Models (LLMs), focusing on building intelligent tooling to simplify and enhance RTL design workflows.

Education

The Neotia University, B. Tech. in Computer Science & Engineering — Sep 2020 – Jun 2024

- CGPA: 9/10

Jhapardah Duke Institution, HS Education with PCM — Jan 2018 – Feb 2020

- Percentage: 82

Experience

Project Linked Person, Indian Statistical Institute, Kolkata — Jul 2024 – Present

- Developed a novel framework to generate Assertions using LLMs to support reliable RTL development
- Our work is accepted in ISVLSI 2025

ML Engineer Intern, Xetalabs India, Guwahati — Jan 2024 – Jul 2024

- Created an LLM-powered chat application helping "Northeast Frontier Railway" with quick QA on their notice database
- Developed an **OCR-to-vectorization** pipeline for automated information retrieval from document images

Research

System Verilog Assertion Generation using LLMs — Sep 2024 - Mar 2025

Under Prof. Ansuman Banerjee and Dr. Sumana Ghosh

Agentic LLM automation in EDA — Apr 2025 - Present

Under Prof. Ansuman Banerjee

Projects

LISA: LLM Informed Systemverilog Assertion Generation

- Developed a framework that helps generate SystemVerilog assertions from specification documents
- Implemented novel Chain-of-Thought based prompt and RAG-based vector database to achieve high coverage
- Tools Used: Python, LangChain, OpenAI/Anthropic API

Chat with 'Golpokotha' — Live Demo

- Developed a coding-oriented LLM chatbot using the Mistral 8x7B Mixture-of-Experts model, fine-tuned on custom programming data
- Tools Used: NextJS, Huggingface

Convolution Neural Network Based Student Marking System — GITHUB

- Finetuned a Convolution Neural Network based on the Densenet model with a custom curated dataset consisting of images of students
- Tools Used: Python, Pytorch

Publications

Subhajit Paul, Ansuman Banerjee, Sumana Ghosh. *LISA: LLM-Informed SystemVerilog Assertion Generation with RAG and Chain-of-Thought*. Accepted at **IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2025)**. To appear.

Achievements

38th Rank, Amazon ML Challenge 2023 — 2023

- Secured 38th position among 26000 participants in Amazon ML Challenge 2023